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FIG. 3A

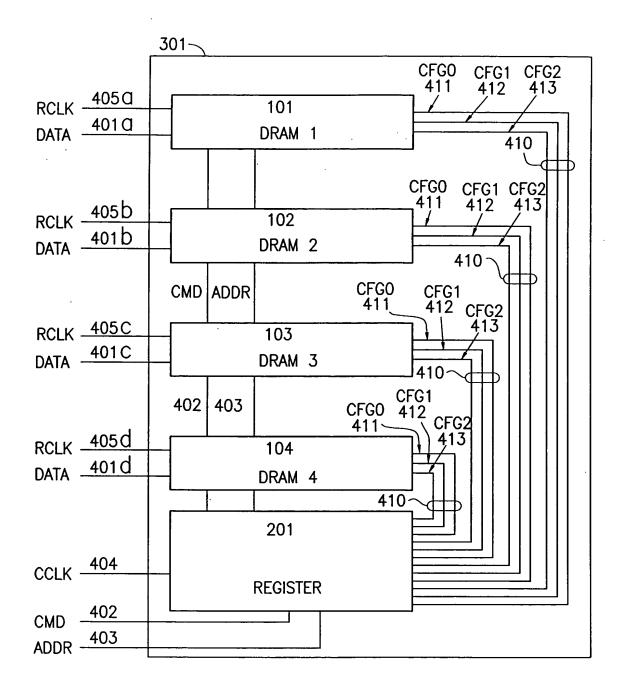
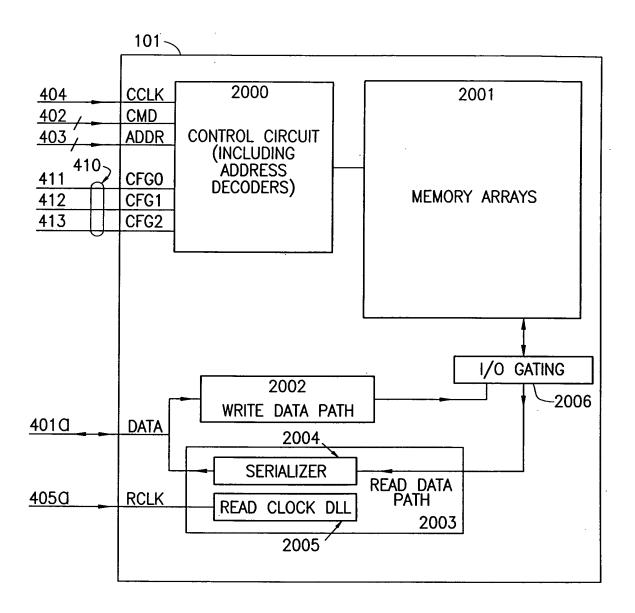
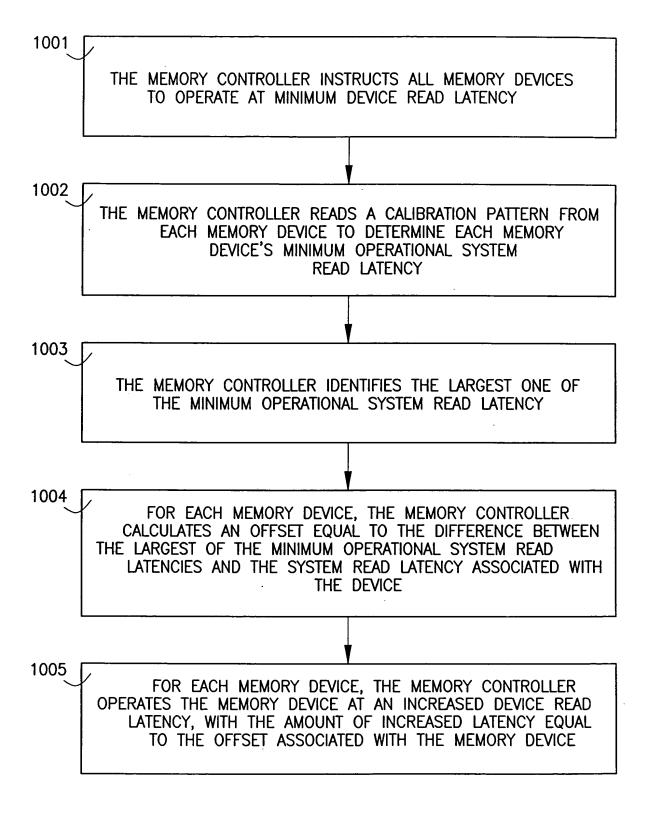


FIG. 3B



DEVICE READ LATENCY	CFG2	CFG1	CFG0
MINIMUM DEVICE READ LATENCY	0	0	0
MINIMUM DEVICE READ LATENCY + 1 CLOCK CYCLE	0	0	1
MINIMUM DEVICE READ LATENCY + 2 CLOCK CYCLES	0	1	0
MINIMUM DEVICE READ LATENCY + 3 CLOCK CYCLES	0	1	1
MINIMUM DEVICE READ LATENCY + 4 CLOCK CYCLES	1	0	0
MINIMUM DEVICE READ LATENCY + 5 CLOCK CYCLES	1	0	1
MINIMUM DEVICE READ LATENCY + 6 CLOCK CYCLES	1	. 1	0
MINIMUM DEVICE READ LATENCY + 7 CLOCK CYCLES	1	1	1



DRAM

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